CLAIMS:

1. An insulated gate semiconductor device, comprising:

a first semiconductor layer of a first conductivity type having first and second main surfaces;

a second semiconductor layer of a second conductivity type with a low impurity concentration provided on the first main surface of said first semiconductor layer;

a third semiconductor layer of the second conductivity type with an impurity concentration higher than the impurity concentration of said second semiconductor layer and provided in close contact on a surface of said second semiconductor layer;

a fourth semiconductor layer of the first conductivity type provided in close contact on a surface of said third semiconductor layer;

a fifth semiconductor layer of the second conductivity type selectively provided in a surface of said fourth semiconductor layer;

a trench having an opening in a surface of said fifth semiconductor layer and having a depth extending through at least said fourth semiconductor layer from the surface of said fifth semiconductor layer;

an insulating film provided on an inner wall of said trench;

a control electrode provided in said trench, facing said fourth semiconductor layer through said insulating film;

a first main electrode provided on the surface of said fourth and fifth semiconductor layers; and

a second main electrode provided on the second main surface of said first

semiconductor layer.

2. The insulated gate semiconductor device according to claim 1, wherein said trench has a depth which extends also through said third semiconductor layer to reach said second semiconductor layer.

3. The insulated gate semiconductor device according to claim 1, wherein said trench has a depth which stays in said third semiconductor layer.

4. The insulted gate semiconductor device according to claim 3, wherein a thickness of said third semiconductor layer between a bottom of said trench and said second semiconductor layer is not more than a critical thickness at which a rapid decrease appears in a breakdown voltage of said insulated gate semiconductor device with an increase in the thickness.

5. The insulated gate semiconductor device according to claim 1, wherein said second semiconductor layer extends through said first semiconductor layer and is partially exposed in the second main surface of said first semiconductor layer.

6. The insulated gate semiconductor device according to claim 1, wherein a sixth semiconductor layer of the second conductivity type with an impurity concentration higher than the impurity concentration of said second semiconductor layer is provided between said first semiconductor layer and said second semiconductor layer.

7. The insulated gate semiconductor device according to claim 6, wherein said sixth semiconductor layer extends through said first semiconductor layer and is partially exposed in the second main surface of said first semiconductor layer.

8. The insulated gate semiconductor device according to claim 1, wherein said trench includes a plurality of unit trenches arranged side by side, and

a part of the exposed surface of said fourth semiconductor layer is provided being interposed between said unit trenches adjacent each other.

9. The insulated gate semiconductor device according to claim 8, wherein the exposed surface of said fourth semiconductor layer is divided into a plurality of unit exposed surfaces by a part of said fifth semiconductor layer, the plurality of unit exposed surfaces being arranged alternately with part of said fifth semiconductor layer along said trench.

10. A method of manufacturing an insulated gate semiconductor device, comprising:

a substrate forming step of forming a semiconductor substrate defining first and second main surfaces and having a first semiconductor layer of a first conductivity type and a second semiconductor layer of a second conductivity type with a low impurity concentration, said first semiconductor layer being exposed in said first main surface and said second semiconductor layer being exposed in said second main surface;

a first implantation step of implanting and diffusing impurity of the second conductivity type to an impurity concentration higher than the impurity

concentration of said second semiconductor layer into said second main surface of said semiconductor substrate to form a third semiconductor layer of the second conductivity type in a surface portion of said second semiconductor layer;

a second implantation step of implanting and diffusing impurity of the first conductivity type in a surface of said third semiconductor layer to form a fourth semiconductor layer of the first conductivity type in a surface portion of said third semiconductor layer;

a third implantation step of forming a resist pattern selectively having an opening in a surface of said fourth semiconductor layer on the surface of said fourth semiconductor layer and implanting and diffusing impurity of the second conductivity type using the resist pattern as a mask to selectively form a fifth semiconductor layer of the second conductivity type in a surface portion of said fourth semiconductor layer;

a first removing step of forming a shield film having an opening surrounding a part of a surface of said fifth semiconductor layer on the surface of said fourth semiconductor layer and the surface of said fifth semiconductor layer and selectively removing said semiconductor substrate using the shield film as a mask to form a trench with a depth extending through at least said fourth semiconductor layer, and removing said shield film after that;

a first step of forming an insulating film on surfaces of said trench, said fourth semiconductor layer and said fifth semiconductor layer;

a first provision step of providing a conductor on said insulating film so as to fill said trench;

a second removing step of uniformly removing said provided conductor to the opening of said trench so as to leave the conductor in said trench as a control

electrode;

a second provision step of providing an insulating layer on the surface of said insulating film and a surface of the conductor buried in said trench;

a third removing step of forming a resist pattern having an opening surrounding the surface of said fourth semiconductor layer and a part of the surface of said fifth semiconductor layer on a surface of said insulating layer and selectively removing said insulating layer and said insulating film using the resist pattern as a mask;

a step of providing a conductor on the surfaces of said fourth and fifth semiconductor layers exposed by said third removing step to form a first main electrode; and

a step of providing a conductor on said first main surface of said semiconductor substrate to form a second main electrode.

11. The method of manufacturing the insulated gate semiconductor device according to claim 10, wherein, in said first removing step, said trench is formed with a depth extending also through said third semiconductor layer.

12. The method of manufacturing the insulated gate semiconductor device according to claim 10, wherein said trench is formed with a depth which stays in said third semiconductor layer in said first removing step.

13. The method of manufacturing the insulated gate semiconductor device according to claim 12, wherein, in said first removing step, said trench is formed with a depth so that a thickness of said third semiconductor layer between the

bottom of said trench and said second semiconductor layer is not more than a critical thickness at which a rapid decrease appears in a breakdown voltage of said insulated gate semiconductor device with an increase in the thickness.

14. The method of manufacturing the insulated gate semiconductor device according to claim 10, wherein said substrate forming step comprises the steps of;

preparing a semiconductor substrate body of the first conductivity type having two main surfaces, and

providing a semiconductor layer of the second conductivity type with a low impurity concentration by the epitaxial growth on one of the main surfaces of said semiconductor substrate body to form said second semiconductor layer.

15. The method of manufacturing the insulated gate semiconductor device according to claim 10, wherein said substrate forming step comprises the steps of;

preparing a semiconductor substrate body of the second conductivity type with a low impurity concentration having two main surfaces,

implanting impurity of the first conductivity type into one of the main surfaces of said semiconductor substrate body; and

diffusing said impurity implanted into said one main surface to form said first semiconductor layer of the first conductivity type.

16. The method of manufacturing the insulated gate semiconductor device according to claim 15, wherein said step of implanting the impurity of the first conductivity type comprises the steps of,

forming a resist pattern having a selectively formed opening on said one

main surface of said semiconductor substrate body, and

selectively implanting impurity of the first conductivity type into said one main surface of said semiconductor substrate body using said resist pattern formed on said one main surface as a mask.

17. The method of manufacturing the insulated gate semiconductor device according to claim 10, wherein said semiconductor substrate formed in said substrate forming step further comprises a sixth semiconductor layer of the second conductivity type with a high impurity concentration interposed between said first semiconductor layer and said second semiconductor layer.

18. The method of manufacturing the insulated gate semiconductor device according to claim 17, wherein said substrate forming step comprises the steps of;

preparing a semiconductor substrate body of the first conductivity type having two main surfaces, and

sequentially forming said sixth semiconductor layer and said second semiconductor layer by the epitaxial growth on one of the main surfaces of said semiconductor substrate body.

19. The method of manufacturing the insulated gate semiconductor device according to claim 17, wherein said substrate forming step comprises the steps of;

preparing a semiconductor substrate body of the second conductivity type with a low impurity concentration having two main surfaces,

forming said sixth semiconductor layer by implanting impurity of the second conductivity type and then diffusing on one of the main surfaces of said

semiconductor substrate body, and

implanting and then diffusing impurity of the first conductivity type in a surface of said sixth semiconductor layer to form said first semiconductor layer.

20. The method of manufacturing the insulated gate semiconductor device according to claim 19, wherein said step of forming said first semiconductor layer comprises the steps of;

forming a resist pattern having a selectively formed opening on the surface of said sixth semiconductor layer,

selectively implanting impurity of the first conductivity type into the surface of said sixth semiconductor layer using said resist pattern formed on the surface of said sixth semiconductor layer as a mask, and

diffusing said impurity selectively implanted into the surface of said sixth semiconductor layer.

21. The method of manufacturing the insulated gate semiconductor device according to claim 10, wherein, if the impurity concentrations in said second semiconductor layer, said third semiconductor layer and said fourth semiconductor layer are taken as C_2, C_3, C_4, respectively, said first implantation step and said second implantation step are carried out so that the relation thereof is $C_2<C_3<C_4$.